Claims

What is claimed is:

1. A system comprising:
   a pulse width modulation (PWM) controller,
      wherein the PWM controller provides a first output for a high-side PWM signal and a second output for a low-side PWM signal; and
   an output stage,
      wherein the output stage is configured to receive the high-side signal from the first PWM controller output and the low-side signal from the second PWM controller output, and
      wherein the high-side signal is coupled to a high-side transistor through a pulse transformer.

2. The system of claim 1, further comprising a high-side programmable delay unit configured to delay the high-side signal by a first programmable amount and a low- side programmable delay unit configured to delay the low-side signal by a second programmable amount.

3. The system of claim 2, wherein the high-side programmable delay unit and the low-side programmable delay unit are integrated into the PWM controller.

4. The system of claim 2, wherein the high-side programmable delay unit is digitally programmable to adjust the first programmable amount and the low-side programmable delay unit is digitally programmable to adjust the second programmable amount.

5. The system of claim 2, wherein the PWM controller is configured to adjust overlap of pulses of the high-side signal and the low-side signal by adjusting at least one of the first and second programmable amounts.

6. The system of claim 1, wherein the PWM controller is configured to produce a pulse as the high-side signal at the first PWM controller output.

7. The system of claim 6, wherein the output stage further comprises a low-voltage driver, and wherein the low-voltage driver amplifies the pulse and transmits the amplified pulse to the pulse transformer.

8. The system of claim 1, wherein the output stage further comprises a third transistor, wherein the third transistor is coupled to receive the low-side signal and wherein the third transistor is configured to turn off the high-side transistor when the low-side signal is asserted.

9. The system of claim 8, wherein the low-side signal is coupled to the third transistor through one or more level shifting capacitors.

10. The system of claim 8, wherein the PWM controller is configured to provide a pulse at the second PWM controller output upon shutdown of the transistors.

11. The system of claim 1, wherein the low-side signal is coupled to a low-side transistor through one or more level shifting capacitors

12. An output stage for a PWM amplifier comprising:

a first input for a high-side PWM signal and a second input for a low-side PWM signal;

a first transistor coupled to receive the high-side PWM signal and a second transistor coupled to receive the low-side PWM signal;

a pulse transformer coupled between the first input and the first transistor; and

a third transistor coupled between the second input and the first transistor;

wherein when a pulse is received at the first input, the first transistor is turned on, and when a pulse is received at the second input, the second transistor is turned on and the first transistor is turned off

13. The system of claim 12, wherein the low-side signal is coupled to the third transistor through one or more level shifting capacitors.

14. The system of claim 12, wherein the PWM controller is configured to provide a pulse at the second PWM controller output upon shutdown of the transistors.

15. The system of claim 12, further comprising one or more level shifting capacitors coupled between the second input and the second and third transistors.